IN THE CLAIMS:

Presented below is a complete list of claims with amendments marked up:

1. (Currently Amended) An apparatus comprising:

an interface to couple to a data bus, the data bus to transfer data between the interface and one or more memory devices;

a logic unit to generate a command occurrence signal to identify when a command signal is issued, wherein a plurality of data transfer operations on one of the one or more memory devices are completed in response to the command occurrence signal, a transition of a flag signal, and a chip select signal corresponding to the one memory device.

~~a controller to couple to a data bus and to a plurality of devices to transfer data between the devices and the data bus in response to a command signal, said controller to generate a chip select signal to select a particular device from the plurality of devices to respond to the command signal; and~~

~~a logic unit coupled to generate a command occurrence signal based on timing of chip select signals to identify when command signals occur, the command occurrence signal to be asserted prior to the chip select signals to allow a flag signal to complete a data transfer.~~

2. (Currently Amended) The apparatus of claim 1, wherein the command occurrence signal, chip select signal and the flag signal are ~~coupled to~~captured by a table entry in the ~~particular~~ one memory device, so that an indication of a presence of all three signals causes a trigger signal to be generated in the ~~particular~~ one memory device to ~~execute~~ complete the plurality of data transfer operations.

3. (Currently Amended) The apparatus of claim 2, wherein the table entry is to be cleared after the one memory device receiving the flag signal to allow said table entry to receive a next set of command occurrence, chip select, and flag signals to determine if the trigger signal is to be generated for the ~~particular~~ one memory device with the next set of command occurrence, chip select and flag signals.

4. (Currently Amended) The apparatus of claim 3, wherein the transition of the flag ~~signal to indicate timing of the data transfer occurs with~~is a positive ~~and~~ transition or a negative transitions ~~of the flag signal~~.

5. (Currently Amended) The apparatus of claim 3, wherein ~~said memory is a dynamic random access memory, DRAM~~the one or more memory devices include one or more dynamic random access memories (DRAM).

6. (Currently Amended) The apparatus of claim 1, wherein the command signal is a read or write command signal for ~~a~~ the one memory device.

7. (Currently Amended) An apparatus comprising:

a memory, ~~to~~ coupled to a data bus, to transfer data between said memory and the data bus in response to a command signal ~~received~~ to initiate a plurality of data transfer operations~~and a flag signal received to complete the data transfer~~, said memory to operate as one of a plurality of memories in which a chip select signal selects said memory from the plurality of memories, ~~and~~ wherein ~~a flag signal operating in timing order with a command occurrence signal, which is based on timing of chip select signals to the plurality of memories, indicates timing when the data transfer is to occur following the~~

~~command occurrence signal, the command occurrence signal to be asserted prior to the chip select signals to allow the flag signal to complete the data transfer~~the plurality of data transfer operations are initiated in response to a command occurrence signal; and

a timing unit, coupled to the memory, to receive the command occurrence signal, a flag signal, and the chip select signal, said timing unit to generate a trigger signal in response to the flag signal to ~~execute~~ complete the plurality of data transfer operations~~,~~ if the command occurrence signal and the chip select signal indicate that said memory is selected ~~for the data transfer~~.

8. (Original) The apparatus of claim 7 wherein the command signal is a read command or write command.

9. (Original) The apparatus of claim 8 wherein the command occurrence signal is a rank select signal to select a rank of memory containing the memory to be selected by the chip select signal.

10. (Currently Amended) The apparatus of claim 9, wherein said timing unit includes table entries to maintain a record of the rank select signal, the chip select signal, and the flag signal, so that a rank entry is to be set when the rank select command is present, a chip select entry is to be set when the chip select signal is present, and the flag entry is to be set when the flag signal is present, the trigger signal is to be generated to ~~execute~~ complete the plurality of data transfer operations when all three respective entries are set.

11. (Currently Amended) The apparatus of claim 10, wherein the respective table entries are to be cleared after the memory receiving the flag signal to allow the entries to receive a next set of rank select, chip select, and flag signals.

12. (Currently Amended) The apparatus of claim 11, wherein the transition of the flag signal ~~to indicate timing of the data transfer occurs with~~is a positive ~~and~~ transition or a negative transitions ~~of the flag signal~~.

13. (Currently Amended) The apparatus of claim 12, wherein said memory is a ~~dynamic random access memory, DRAM~~dynamic random access memory (DRAM).

14. (Currently Amended) The apparatus of claim 9, wherein said timing unit includes a table having entries arranged in a queue to maintain a record of occurrences of the rank select, chip select, and ~~the~~ flag signals, so that subsequent occurrences of all three signals is to be recorded.

15. (Original) The apparatus of claim 14 further includes a first pointer to point to a next set of entries after recording the occurrence of the rank select and chip select signals; and a second pointer to point to the next set of entries after recording the occurrence of the flag signal.

16. (Currently Amended) The apparatus of claim 14, wherein said memory is a ~~dynamic random access memory,~~dynamic random access memory (DRAM).

17. (Currently Amended) A system comprising:

a controller to generate a command signal, ~~to initiate a data transfer in response to the command signal, said controller to generate~~ a chip select signal, a rank select signal, and a flag signal associated with the command signal;

a bus coupled to said controller; and

a plurality of memories coupled to the controller via the bus, said bus to transfer data between ~~said~~ one of the plurality of memories and the bus in response to the command signal ~~generated by said controller~~, the one of said plurality of memories being selected by the chip select signal for ~~the~~ a data transfer, wherein ~~in which the flag signal times the execution of the data transfer and the rank select signal times the occurrence of the command signal,~~ the rank select signal ~~to be~~ is asserted prior to the chip select signal to allow the flag signal to complete the data transfer.

18. (Currently Amended) The system of claim 17, wherein one of ~~said~~ the plurality of memories includes a timing unit, ~~in which~~ having a table of entries ~~in the timing unit maintains~~ to maintain a record of the rank select signal, the chip select signal, and the flag signal, so that a rank select entry is to be set when the command signal is a read or write command, a chip select entry is to be set when the chip select signal is present, and the flag entry is to be set when the flag signal is present, and a trigger signal is to be generated to ~~execute~~ complete the data transfer when all three respective entries are set.

19. (Currently Amended) The system of claim 18, wherein the respective ~~table~~ entries are to be cleared after the one of the plurality of memories receiving the flag signal to allow the entries to receive a next set of rank select, chip select, and flag signals.

20. (Currently Amended) The system of claim 19, wherein the transition of the flag signal ~~to indicate timing of the data transfer occurs with~~is a positive ~~and~~ transition or a negative transitions ~~of the flag signal~~.

21. (Currently Amended) The system of claim 19, wherein ~~said~~ the plurality of memories include one or more dynamic random access memories (DRAM)~~memory is a dynamic random access memory, DRAM~~.

22. (Currently Amended) A method comprising:

issuing a command signal to perform a read or write operation;

issuing a chip select signal to select a ~~particular~~ memory device from a plurality of memory devices to perform a data transfer for the read or write operation;

issuing a command occurrence signal to identify when the command signal is ~~generated~~issued, the command occurrence signal being ~~generated~~ issued prior to the chip select signal;

generating a flag signal ~~subsequently~~ in response to the issuing of the command signal ~~to complete the data transfer~~; and

capturing occurrences of the command occurrence signal, chip select signal and the flag signal in ~~a~~ the memory device; and

generating a trigger signal when the command occurrence, chip select, and flag signals present are captured ~~for~~ in the memory device, the trigger signal to ~~execute~~ complete the data transfer ~~to complete~~for the read or write operation in the memory device.

23. (Original) The method of claim 22 wherein the command occurrence signal is asserted one clock period prior to the chip select signal being asserted.

24. (Currently Amended) The method of claim 23, wherein said capturing the signals ~~are achieved by~~comprises setting entries on occurrences of the signals.

25. (Original) The method of claim 24 further including the clearing of the entries after occurrence of the flag signal.

26. (Currently Amended) The method of claim 23, wherein ~~said capturing of the signals is performed in a dynamic random access memory, DRAM~~the plurality of memory devices include one or more dynamic random access memories (DRAM).